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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/020,741 | 12/12/2001 | Charles H. Dennison | 2269-3259.1US | 2283 |

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| EXAMINER | |
|---|---|
| NGUYEN, TUAN H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2813 | |

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/020,741 | DENNISON ET AL. | |
| | Examiner | Art Unit | |
| | Tuan H. Nguyen | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *61-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *61-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Terminal Disclaimer*

The terminal disclaimer filed on 1/26/2004 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. RE 38,049 has been reviewed and is accepted. The terminal disclaimer has been recorded.

The double patenting rejection has been withdrawn in view of the terminal disclaimer dated 1/26/2004.

### *Claim Rejections - 35 USC § 112*

The 35 U.S.C 112 rejection has been withdrawn in view of the amendment dated 1/26/2004.

### *Oath/Declaration*

The reissue oath/declaration filed with this application is defective because it fails to contain a statement that all errors which are being corrected in the reissue application up to the time of filing of the oath/declaration arose without any deceptive intention on the part of the applicant. See 37 CFR 1.175 and MPEP § 1414.

In accordance with 37 CFR 1.175(b)(1), a supplemental reissue oath/declaration under 37 CFR 1.175(b)(1) must be received before this reissue application can be allowed.

Claims 61-71 are rejected as being based upon a defective reissue declaration under 35 U.S.C. 251. See 37 CFR 1.175. The nature of the defect is set forth above.

Receipt of an appropriate supplemental oath/declaration under 37 CFR 1.175(b)(1) will overcome this rejection under 35 U.S.C. 251. An example of acceptable language to be used in the supplemental oath/declaration is as follows:

> "Every error in the patent which was corrected in the present reissue application, and is not covered by a prior oath/declaration submitted in this application, arose without any deceptive intention on the part of the applicant."

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 61-71 are rejected under 35 U.S.C. 102(e) as being anticipated by Gonzalez et al.(cited by applicant).

Gonzalez et al., figs. 1-15 and related text on col. 5-9 discloses the claimed method for forming a capacitor including the steps of providing a first insulating 40 of BPSG having a first etch rate, and forming an opening 55 into the first insulating layer 40 thereby forming a container on the substrate 3 (fig. 3, col. 6, fifth paragraph); forming a generally conformal first conductive layer 60 over the first insulating layer 40 and in the opening 55 of the container; forming a second insulating layer 65 of oxide having a second etch rate, above the first conductive layer 60 (fig. 4, col. 6, sixth paragraph); removing at least a portion of the second insulating 65 through the use of CMP until an upper portion of the first conductive layer 60 is exposed; and removing at least a portion of the first conductive layer 60 until the first insulating 40 is exposed, thereby forming a conductive container having inner and outer walls (fig. 7B, 8B, col. 7, fifth paragraph).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 61-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. in view of Gonzalez et al. (both cited by applicant).

Kwon et al., figs. 2-4 and text on col. 2-3 discloses substantially the claimed process for forming a capacitor including the steps of forming a conformal first conductive layer 48 over the first insulating layer 46 of oxide having a first etch rate and in the container 54; forming a second insulating layer 50 of photoresist having a second etch rate over the first conductive layer 48; removing the second insulating layer 50 until an upper portion of the first conductive layer 48 is exposed (fig. 4C); removing at least a portion of the upper portion of the first conductive layer 48 until the first insulating layer 46 is exposed, thereby forming a conductive container having inner and outer walls (fig. 4D).

Kwon et al., fig. 4C and text on col. 3, lines 21-25 generally discloses the use of etch-back process for planarizing the second insulating layer until the first conductive layer 48 is exposed. Kwon et al. does not particularly teach the use of CMP for etch-back process.

Gonzalez et al., in a related method for forming a capacitor as shown particularly in figs. 7A, 7B and text on col. 7, fourth and fifth paragraphs, teaches the use of either wet etching or chemical mechanical planarization method for etching back the layers for forming a conductive container having inner and outer walls.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used CMP as an alternative method as suggested by Gonzalez et al. in the etch-back process of Kwon et al. for planarizing the semiconductor surface, since they are well-known alternative methods for planarizing the semiconductor surface in the semiconductor art.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Response to Arguments***

Applicant's arguments filed 1/26/04 have been fully considered but they are not persuasive.

- With respect to 35 U.S.C. 102(e) anticipation rejection based on U.S. Patent No. 5,150,276 to Gonzalez et al., each and every elements as set forth in the instant claim is found in the reference to Gonzalez et al. as explained above.

The instant independent claims 61, 66, and 71 which recite a process for fabricating a capacitor on a substrate comprising the step of "removing at least a portion of said second insulating layer through the use of chemical mechanical planarization until an upper portion of said first conductive layer is exposed." do not require that the CMP of a second insulating layer ceases once an upper layer of the first conductive

layer is exposed, and preclude the further process of CMP to remove the first conductive layer as shown in Gonzalez et al., fig. 7B.

Contrary to the Applicant argument in his Remarks page 7, second and third paragraph that "Gonzales et al. does not disclose a process for fabricating a capacitor on a substrate, which comprises removing at least a portion of a second insulating layer through use of chemical mechanical planarization (CMP) until an upper portion of the first conductive layer is exposed.".

Fig. 7A clearly shows at least a portion (pointed portion) of the second insulating layer 65 formed above the first conductive layer 60 before it is subjected to CMP, and fig. 7B shows the planarized structure after it was subjected to CMP wherein at least a portion of the second insulating layer 65 (pointed portion as shown in fig. 7A) is removed until an upper portion of the first conductive layer 60 is exposed (and further removed which is not precluded by the instant claims).

- With respect to 35 U.S.C. 103(a) Obviousness Rejection.

Contrary to the applicant's argument in his Remarks, page 8, fourth paragraph that "forming a second insulating layer above a first conductive layer" as recited, requires that a second insulating layer be formed over the entire first conductive layer, and not a portion of said layer". Note that "above" does not means "over the entire" or "fully cover" as contended by the applicant. Secondly, "removing at least a portion of said second insulating layer through use of chemical mechanical planarization until an upper portion of said first conductive layer is exposed." does not require stopping the CMP process once the upper layer of the first conductive layer is reached or exposed.

The term "until... exposed" does not require the process has to be ceased, and the examiner is having problem of finding the term "cease" in the instant claims.

Moreover, In Kwon et al. reference, second insulating layer 50 is formed over the entire first conductive layer 48 and subsequently etched back until the first conductive layer 48 disposed on top of the second oxide layer 46 is exposed (see col. 3, lines 21-25). Figure 4C shows only portion of second insulating layer 50 left after etch-back process. Not "second photoresist is formed over the first polysilicon layer 48 to partially cover the polysilicon layer 48." as alleged by applicant on page 8, last two paragraphs. By disclosing etch-back process, Kwon et al. leave it open to any etching process, and CMP is a well-known alternated process in semiconductor processing art as suggested by Gonzales et al. for etching back the layer. It would have been obvious to that skilled artisan to have used CMP as suggested by Gonzales et al. in Kwon et al. etch-back process since it is well-known alternative method for planarizing the layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is 571-272-1694. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan H. Nguyen
Primary Examiner
Art Unit 2813